AF/2823 ✓IFW

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/034,723
Filing Date	January 3, 2002
First Named Inventor	Gregory C. DeSalvo
Art Unit	2823
Examiner Name	Julio J. Maldonado
Attorney Docket Number	AFD 643

Total Number of Pages in this Submission: 4

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts / Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to a Group (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) *(please identify below):*

Remarks

RECEIVED JUL 30 2004 OIPE/JCMS

SIGNATURE OF APPLICANT, ATTORNEY OR AGENT

Firm *or* Individual Name	GERALD B. HOLLINS
Signature	Gerald B Hollins
Date	21 July 2004

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name: Gerald B Hollins GERALD B. HOLLINS

Signature: Gerald B Hollins Date: 21 July 2004

FEE TRANSMITTAL for FY 2004

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 330.00

Complete if Known	
Application Number	10/034,723
Filing Date	January 3, 2002
First Named Inventor	Gregory C. DeSalvo
Examiner Name	Julio J. Maldonado
Group Art Unit	2823
Attorney Docket Number	AFD 685

METHOD OF PAYMENT

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None
☒ Deposit Account

Deposit Account Number: AF 01-0465

Deposit Account Name: Department of the Air Force

The Commissioner is authorized to: *(check all that apply)*

☒ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility Filing Fee	
1002	340	2002	170	Design Filing Fee	
1003	530	2003	265	Plant Filing Fee	
1004	770	2004	385	Reissue Filing Fee	
1005	160	2005	80	Provisional Filing Fee	

SUBTOTAL (1) $ 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		- 20** =		x	18	=	0
Indep. Claims		- 3** =		x	86	=	0
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 0

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Code	Large Entity Fee ($)	Small Entity Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner Action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) $ 330.00

SUBMITTED BY

Complete (if applicable)

Typed or Printed Name	GERALD B. HOLLINS	Registration. No.	25,452	Telephone	(937) 255-2838
Signature	Gerald B Hollins			Date	20 July 2004
Typed or Printed Name		Registration. No.		Telephone	
Signature				Date	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/034,723
Applicant(s)	:	Gregory C. DeSalvo et al.
Filed	:	January 3, 2002
Title	:	STIFFENED BACKSIDE FABRICATION FOR MICROWAVE RADIO FREQUENCY WAFERS
TC/AU	:	2823
Examiner	:	Julio J. Maldonado
Docket No.	:	AFD 459

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

BRIEF ON APPEAL

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

This is an appeal from the Final Rejection dated April 07, 2004 in the above captioned application. An oral hearing is not requested.

(1) Real Party in Interest

The captioned appealed application is assigned to the Government of the United States as represented by the Secretary of the Air Force at U.S. Patent and Trademark Office Assignment Division Reel/Frame 012580/0668 dated February 4, 2002.

(2) Related Appeals and Interferences

There are no related Appeals or Interferences.

(3) Status of Claims

Method claims 1-9, 22-25 and 27-37 are pending in the application and each stand as being Finally Rejected; these are the claims under appeal. Claims 1, 22 and 31 of this group are independent claims. Non-Elected apparatus claims 10-21 of the application and claim 26 have been canceled.

(4) Status of Amendments

There are no outstanding amendments to the application. No amendment was filed after the Final Rejection.

(5) Summary of Invention

The invention concerns a method for achieving a thinned wafer microwave radio frequency transistor or integrated circuit (FIG. 2 and FIG. 3 in the application) having desirable transmission line and other thin wafer electrical characteristics and desirable heat conductivity all in combination with a backside support and rigidizing structure (204 and 206 in FIG. 2 and FIG. 3, 400 and 402 in FIG. 4) providing physical strength needed for wafer scale handling and processing with reduced breakage. The wafer (214) is additionally provided with a backside ground plane (304, 308) and with via hole or via region (105) electrical conductors (216) as needed for low electrical impedance radio frequency and microwave integrated circuit use (see 105 and 106 in FIG. 5). The via holes are also arranged to provide a wafer thickness measurement function (page 9, line 24) during processing. Selective backside etching of the wafer in the presence of both patterned and processing fixture-provided masking provides a residual grid (204 and 206 in FIG. 2 and FIG. 3, 400 and 402 in FIG. 4) of interconnected backside support members combining to make the thinned wafer (214) significantly more rugged and less damage susceptible (page 14, line 10) while in the integral wafer state than is possible with conventional thin wafer gross processes such as grinding. The backside support structure (204 and 206 in FIG. 2 and FIG. 3, 400 and 402 in FIG. 4) may be excluded or removed during subsequent wafer dicing where the inherently small individual die size (316 in FIG. 3) affords such die strength as to enable conventional handing for packaging purposes (page 11, line 3). The invention is made practical by the use of a rapid and favorable-surfaces-achieving etching process (page 7, line 6) on the wafer backside.

(6) Issues

A central issue in this appeal relates to whether claims 1-9, 22-25 and 27-37 are patentable in view of 35 U.S.C. 103(a) over the variously combined primary references of Hayama et al. (U.S. 6,440,882) and Morcom et al. (U.S. 6,162,702; particularly FIG. 5 and FIG. 6) with various considerations of the secondary references of Kohno et al. (U.S.

6,358,762), Yamada et al. (U.S. 6,297,131) and Matsunami (U.S. 5,463,246). Herein these references are referred to as the patents of Hayama et al., Morcom et al., Kohno et al., Yamada et al. and Matsunami.

(7) Grouping of Claims

The Examiner has assigned applicants' rejected claims to five different groups as follows:

1. A first group inclusive of claims 1-7, 9, 31-34 and 37 and rejected in view of a combination of the Hayama et al. and Morcom et al. references.

2. A second group inclusive of claims 8 and 35 and rejected in view of a combination of the Hayama et al., Morcom et al. and Kohno et al. references.

3. A third group inclusive of claims 22, 30 and 36; 23, 24 and 28 and rejected in view of a combination of the Hayama et al., Morcom et al. and Yamada et al. references.

4. A fourth group inclusive of claim 27 and rejected in view of a combination of the Hayama et al., Morcom et al., Yamada et al. and Matsunami references.

5. A fifth group inclusive of claim 29 and rejected in view of a combination of the Morcom et al., and an earlier Goldstein references. This rejection is believed to be erroneous in view of a purported reliance on the now superceded Goldstein reference as is noted below herein.

Applicants herein present argument focusing on the Hayama et al. and the Morcom et al. primary reference patents and their combination as appear an essential part of each Examiner claim group rejection. A finding of merit in this argument is submitted to result in all pending claims of the application being patentable. From this perspective therefore the claims in the application stand or fall together.

In addition applicants present specific distinction arguments relating to claims 1, 4, 22, 23, 24, 30, 31, 33 in the application. A finding of merit in one or more of these specific distinction arguments may result in specific claims of the application, but possibly not all claims, being patentable. From this perspective therefore the claims in the application do not stand or fall together. Excepting for these specific distinction possibilities therefore the claims in the application are believed to stand or fall together.

(8) Argument

The captioned application has been twice rejected and stands as being "Finally Rejected". The Rejection is based on 35 U.S.C. 103(a) obviousness and supported by the newly cited primary reference of Hayama et al., U.S. 6,440,822, in combination with the previously cited primary reference of Morcom et al., U.S. 6,162,702, and the secondary references of Matsunami, U.S. 5, 463,246, Yamada et al., 6,297,131 and Kohno et al. 6,358,762. Applicants herein present responses inclusive of distinction on the merits especially relating to the Hayama et al. and Morcom et al. references.

Applicants' present appeal brief response includes a plurality of topics that are each provided with Roman numeral identification and are generally each inclusive of a plurality of sub topics. The first two of these topics relate to the primary references and the third to the combination of these references. Additional of these Roman numeral topics address legal considerations and miscellaneous matters

I. Merits of the Hayama et al. Reference

Applicants understand this patent to be concerned with fabricating a Monolithic Microwave Integrated Circuit (a MMIC) typically inclusive of a substrate with a series of saw cuts, metal layers, metal sidewall coverings and substrate thinning achieved by mechanical polishing or grinding--as accomplished through use of a wax bonded "support" or carrier. Notably, the underlying purpose of the Hayama et al. patent appears to be the achievement of metal sidewall coverings for an inert substrate material such as sapphire; discussion relating to this purpose appears subsequently herein. Most of these details are recited in the SUMMARY OF THE INVENTION and the remainder in the first five paragraphs of the DESCRIPTION OF THE PREFERRED EMBODIMENT portions of the Hayama et al. patent. Applicants' believe the invention in their application is distinguished in several significant respects from the structure disclosed in the Hayama et al. patent and from the asserted combination of this structure with the Morcom et al. patent.

1. A first of these distinctions concerns applicants' clear recitation in the rejected independent claims 1, 22 and 31 of the application of wafer via-holes. In the Final Rejection the Examiner asserts, in numbered paragraph 4, that the dicing saw trench cuts 2 in the Hayama et al. structure meet applicants' recitation of such wafer via-holes.

Applicants respectfully disagree with this assertion by the Examiner. A via-hole is known in the electronic art as a controlled dimension precisely located usually circular and

etched hole connecting different layers of a semiconductor device. In many instances via-holes are carefully disposed directly below a transistor element such as a field effect transistor source, gate or drain element (as appears in applicants' FIG. 5 drawing for example) or below a junction transistor emitter, base or collector element. Such via holes serve the purpose of achieving a low impedance interconnection of that transistor element with a ground plane or a power supply conductor or some other conductor residing in a different layer of the device. Applicants' use of the expression "via-hole" is in agreement with this knowledge and practice in the electronics art.

The dicing saw trench 2 in the Hayama et al. patent is distinguishable from a true via-hole in at least its shape, in its function, in its dimensions and in its manner of accomplishment. Via-holes are usually circular and of some tens of micrometers in diameter while a dicing saw cut is necessarily larger and of at least the 100 to 400 micrometers width recited at column 4, line 30 of the Hayama et al. patent--because such dimension is necessary to provide structural integrity in the dicing saw blade.

Via-holes may be disposed in any location and in many locations across the surface of a wafer in whatever position is desired for circuit interconnection with a ground plane or power supply bus or between conductors of two different wafer layers. A saw cut or "trench", by its crude often hand guided nature, is however frequently disposed at the edge of a circuit die or "chip" where open space is available and where, as in the Hayama et al. patent, it provides a circuit die segregation function (see Hayama et al. at column 3, line 11 and column 5 line 48 for examples). The length of the saw cut does not appear in the cross sectional drawing views of the Hayama et al. patent; this perhaps explains some confusion on the part of the Examiner in equating the Hayama et al. saw cuts with applicants' via-holes. The least possible length of a saw cut is of course greater than its thickness because of the significant diameter of a saw blade in comparison with its thickness and because of the need for long cut lengths in a die segregation event; such lengths greatly exceed the diameter of a via-hole.

The location of and the dimensions of a via-hole are determined by masking and etching steps performed during a wafer circuit die fabrication sequence. In contrast a saw cut is usually accomplished after the wafer masking and etching sequence is completed (otherwise individual die fabrication is necessary). A saw cut is determined in location and dimension by some form of external dimensional controls. These controls may include a

computer-aided saw control or human guidance for examples. With respect to saw cut dimensions, saw geometry is a significant lower limit consideration.

The absence of via holes in the Hayama et al. reference is of particular interest in the present proceedings since the Hayama et al. patent appears to be included in these proceedings specifically for its disclosure of radio frequency and communications apparatus. The remaining four references relied upon by the Examiner appear significantly removed from the radio frequency signal art.

In summary there is no teaching of the vias or via-holes recited in applicants' rejected claims included in the Hayama et al. reference patent as the Examiner has asserted. This absence raises the suggestion that the Hayama et al. patent at least teaches away from applicants' invention, is non-analogous art with respect to applicants invention, is based on a hindsight view of applicants' invention and that the Examiner fails to consider all of the limitations recited in applicants rejected claims. The legal significance of these conclusions is addressed in a subsequent topic herein.

2. The fabrication of sidewall metal layers is a significant aspect of the Hayama et al. invention, see the Hayama et al. specification commencing at column 1, line 8; column 2, line 66; column 4, line 32 for examples. These sidewall metal layers can function to exclude the need for genuine via-holes in the Hayama et al. device since they may provide something of an electrical path between device layers. The differing location and size of these sidewall layers is however in conflict with the expressly claim-recited via holes of applicants' invention and provides less desirable electrical characteristics especially at microwave radio frequencies. Such differences again suggest the Hayama et al. patent is most fairly classed as non analogous art or a teaching away from applicants' invention.

3. The Hayama et al. patent calls for use of a support 5, for mounting the substrate 1 during processing of one side of the semiconductor device being fabricated i.e., during processing of "the second main surface", see column 2, line 41. This support 5 is needed during ensuing processing in the Hayama et al. device in order to hold segregated circuit die fixed in position notwithstanding separation of the die from the remaining wafer by the saw cut trenches 2 and 7. The Hayama et al. circuit die are held in this fixed position on the support 5 by a layer of wax 6.

Applicants' invention in contrast with the Hayama et al. disclosure employs no support member or wax under the processed wafer. Applicants' wafer is not subdivided until both front side and backside processing have been completed. Nothing in the rejected claims or the specification of the instant application recites the use of a substrate carrier or of wax attachment to such a carrier.

The Hayama et al. presence of wax and segregation of the wafer die would in fact be detrimental to applicants' backside process in the combination asserted by the Examiner. In such a combination applicants' employed ECR or ICP rapid etch would come into undesired contact with die edge surfaces. Moreover, the heat generated during ECR or ICP etching would be precluded from dissipation by both the Hayama et al. small segregated die size and its limited lateral path dissipation and by the low thermal conductivity resulting from wax presence (wax melting is in fact a probable consequence of an ECR or ICP etch) if the Hayama et al. process were used with applicants invention as the Examiner assertions would achieve. Applicants in fact employ a flow of cooling gas over the wafer front side during the ECR or ICP backside etching and the presence of wax is contrary (i.e., destructive) to this practice. These significant differences between applicants' invention and the Hayama et al. process suggest the Hayama et al. patent is most fairly concluded to be non-analogous art, a teaching away with respect to applicants' invention and as tending to destroy the function of applicants invention. Again the legal significance of these conclusions is addressed in a subsequent topic herein.

II. Merits of the Morcom et al. Reference

The Morcom et al. patent concerns semiconductor devices of the "vertical power device" type as are provided with wafer backside stiffening of several possible configurations. These configurations include a ring and rib aided thinned wafer arrangement in which wafer backside material intermediate supporting ring and rib members is removed in order to achieve better thermal and electrical-resistance properties (emphasis added; see Morcom et al. column 3, line 33). The circular rim 9 of the Morcom wafer is formed with the aid of mask elements 4 and 5 and is connected with wafer spanning ribs 6 and 7 that are disposable in a variety of patterns including the simple cross pattern of FIG. 4, the chord disposed pattern of FIG. 5 and the rectilinear grid pattern of FIG. 6. The underlying purpose of the Morcom et al. patent appears to be the achievement of a less fragile semiconductor wafer; discussion relating to this purpose appears

subsequently herein. For present purposes it is significant to note that the Morcom invention, as indicated by the Examiner, does not include disclosure of wafer thickness-traversing via holes nor does it disclose the use of a metallic ground plane element on the wafer backside.

1. With respect to the present proceedings it appears significant that the Morcom et al. patent includes no recitation concerning the processing of microwave or other radio frequency signals and is in fact directed to what appears to be much lower in frequency "vertical power devices". This directed intention is significantly corroborated by the absence of Morcom et al. via holes and ground plane elements. Applicants' invention is in fact strongly influenced by a need to amplify and communicate just such microwave radio frequency signals and therefore includes via elements (with the few milliohms of electrical resistance and small electrical inductance they provide), surface mounted rather than vertically mounted semiconductor devices and chemically achieved wafer thinning as is needed for example to achieve desirable radio frequency transmission line characteristics. The absence of microwave signal considerations in the Morcom et al. patent suggest this patent is itself most fairly classed as non-analogous art or a teaching away from applicants' invention.

2. The use of conventional silicon etching to remove semiconductor material intermediate the grid pattern of the Morcom et al. wafer is another area of significant difference with respect to applicants' invention. Although such conventional etching may be satisfactory in the case of the Morcom et al. silicon semiconductor, such conventional etching is grossly impractical in the case of the microwave materials and the large thickness reductions needed in applicants' invention. Such conventional etching would require many tens of hours, probably 70 to 100 hours, to accomplish for each of applicants' wafers processed. The advent of the faster inductively coupled plasma (ICP) and Electron Cyclotron Resonance (ECR) processes disclosed in applicants' specification and the resulting 90 minute etching time in fact make applicants' invention practical. Even though the Kohno et al. reference relied upon in the Office Actions discusses an ICP process this does not change the fact that the primary reference Morcom et al. patent teaches away from the ICP combination recited in applicants' claims. The Morcom et al. reference is thereby

believed subject to additional non-analogous art, teaching away and destruction of function question as to its appropriateness as a reference against applicants' invention.

3. Applicants additionally question the Examiner's page 5 assertion that portions of the Morcom ridges could perform the function of applicants' vernier marker via hole measuring elements. Applicants' vernier marker via hole measuring elements are via hole diameter and depth measuring structures disposed within the via holes and within the thickness of the semiconductor wafer and include a graduated measurement scale element (all as disclosed in the incorporated by reference U.S. Patent 6,653,214 by a partially different group of applicants' colleagues). Nothing in the Morcom ring and rib structure is capable of achieving the graduated measurement scale element nor the function of via hole diameter measuring (during an etching step) as has been asserted by the Examiner. Moreover the location of the asserted Morcom et al. "measuring" ridges is significantly different from the in-wafer location of applicants' via measuring elements.

Distinguishing details of applicants' vernier marker are recited in the rejected claims of the application including for example claims 4 and 33. Such details do not appear in the Morcom et al. patent nor in other of the Examiner relied upon references. The absence of structure expressly recited in applicants rejected claims in the relied upon references is believed most fairly classed as a failure by the Examiner to consider all of the limitations of a rejected claim and also as an assertion tending to destroy the function of applicants' invention.

III. Merits of the Combined Hayama et al. and Morcom et al. References

Several aspects, in addition to the preceding observations concerning relied upon details of each primary reference individually, are submitted to merit consideration with respect to the Examiner asserted combination of these references.

1. Applicants respectfully submit that there is no viable teaching in suggestion of the asserted combination of the Hayama et al. and Morcom et al. references, as asserted by the Examiner, appearing in the present instance.

2. Applicants additionally submit that there is no viable teaching in suggestion of the asserted combination of the Hayama et al. and Morcom et al. references with any of the Matsunami, Yamada et al. and Kohno et al. references as is also asserted by the Examiner.

3. Discussions relating to these absences of combination teaching appear in topic V below herein.

4. Technical difficulties result from the Examiner asserted combination of the Hayama et al. and Morcom et al. references. Applicants note in this regard that the Hayama et al. specification teaches the use of a substrate "that can hardly be processed by chemical reactions, thereby to improve the characteristics of an MMICC and raise the yield thereof." (emphasis added) see Hayama et al. column 3, lines 1-3. The Hayama et al. substrate of this nature is in fact a sapphire material in each of the four examples disclosed, see column 4, line 25; column 5, line 34; column 6, line 52 and column 8, line 4. Such "can hardly be processed by chemical reaction" characteristic is submitted to include of course the various processes of chemical etching.

According to the combination of the Hayama et al. and Morcom et al. patents asserted by the Examiner however these sapphire substrates "that can hardly be processed by chemical reaction" are nevertheless to be provided with the grid pattern backside appearing in the FIG. 6 drawing of the Morcom et al. patent in order to achieve this Examiner asserted combination and in order to meet applicants rejected claims. Moreover this grid pattern is to be achieved not with the grinding, milling, drilling or laser processes of the Morcom et al. "first method" as recited at Morcom et al. column 2, line 16 but with the column 2, line 56 called–for second or third Morcom et al. methods of "silicon etching" as recited at column 2, line 43 and column 2, line 48. (A semiconductor device die sized grid pattern is of course impossible to achieve with grinding or milling, the grinding wheel or milling cutter is too large.)

Therefore the combination asserted by the Examiner must resort to the very chemical reaction substrate etching that is said by Hayama et al. to be "hardly possible". The asserted combination thus appears to be impossible of achievement i.e., the desired backside patterns are unavailable on the Hayama et al. substantially inert sapphire substrate as the asserted combination would require. The reference combination relied upon by the Examiner is hence submitted to be untenable and its chance of success small. Using other words, the asserted reference combination destroys the structure and the function of one reference, the Morcom et al. patent and its FIG. 6 grid pattern, the very characteristic of Morcom et al. that is relied upon by the Examiner.

An attempt to combine the Hayama et al. and Morcom et al. patents by using the semiconductor substrate and grid pattern of the Morcom et al. patent in a device of the

Hayama et al. type also destroys the function of the Hayama et al. invention since it directly controverts an asserted advantage of the Hayama et al. invention by excluding the "substrate that can hardly be processed by chemical reactions" and hence does not "improve the characteristics of an MMIC and raise the yield thereof." as stated for a sapphire substrate at Hayama et al. column 3, lines 2 and 3, if the Morcom et al. substrate materials were used in the Hayama et al. device. This is also submitted to be an untenable result of the Examiner asserted combination. These difficulties with the asserted combination of references are submitted to be fairly considered as failing to provide a reasonable expectation of success from the asserted combination of references.

5. As discussed in a previous topic herein the Hayama et al. invention is devoid of via-holes connecting wafer layers. The Morcom et al. patent is similarly devoid of such via holes. In view of these absences applicants' claims clearly reciting the use of such via-holes appear arbitrarily rejected without support by relevant prior art. Such rejection is respectfully submitted to fail to consider all of the limitation in the rejected claims and to be in error.

6. The Hayama et al. semiconductor device includes a substrate support element 5 used in the presence of the wax layer 6 to hold saw trench segregated die in position for metal plating and other processing. The Morcom et al. patent incorporates no such substrate support element since die segregation is there contemplated after completion of die processing. A combination of the Hayama et al. and Morcom et al. structures as asserted by the Examiner has difficulty with this substrate support element difference. The Morcom et al. espoused absence of a support element in a Hayama et al. structure poses the difficulty of providing no means for holding the saw trench-segregated die elements in location for metallization or other subsequent processing steps. The Hayama et al. invention would thus be destroyed by such a change. Conversely the addition of a support element in the Morcom et al. structure would make the cardinal element of the Morcom et al. invention, the backside support ring and rib structure, excessive and unnecessary since the support element provides desired wafer-breakage protection.

7. The record of the instant application is respectfully submitted to provide a reasonable basis to question support for a prima facie case of obviousness under 35 U.S.C.

103(a) in view of the rejection having been asserted with respect to a combination of the Morcom et al. and the Goldstein et al. primary references in the first Examiner's Action and then without explanation or plausible teaching to combine references abruptly based on a new combination of the Morcom et al. and Hayama et al. primary references in the second Examiner's Action. Such unexplained switching between references and theory of rejection is respectfully submitted to raise at least an inference of the strongest common thread between rejections being applicants' teachings i.e., the rejections being based on hindsight in view of applicants' invention.

8. The Examiner reliance on section 2144.07 in the Manual of Patent Examining Procedures and the rationale of "Art Recognized Suitability for an Intended Purpose" in support of the asserted combination of the Hayama et al. and Morcom et al. references is respectfully submitted to provide little support for the present 35 U.S.C. 103(a) rejection upon closer consideration of the three cases summarized in section 2144.07. The first of these cases, the U.S. Supreme Court Sinclair case from 1945, involves a reference teaching the same subject matter and the same function as that of the application in question, i.e., a printing ink wet at room temperature but rapid drying at elevated temperature.

The second of these cases involved an application wherein one plastic material was substituted for another in fabricating the same structure, a container. The third of these cases involved an application and a reference differing only with respect to a function, the reference having mechanically operated brakes, the application hydraulically operated brakes. Applicants respectfully submit that at least the structural differences identified between application and references herein as well as the differing problems addressed by the two combined references separate the instant situation from the thrust of these section 2144.07 examples.

IV. Specific Claim and Language Distinctions

Salient recitations in certain of applicants' rejected claims ostensibly merit little consideration by the Examiner yet appear to provide distinction over the prior art relied upon in the final rejection; some of these recitations have been briefly considered previously herein in discussing the primary Hayama et al. and Morcom et al. references however a more complete discussion appears justified.

Even if all of the previously identified difficulties with the Examiner's position of rejection were to be found lacking in merit, the following noted express claim recitations appear to clearly and specifically distinguish over the relied upon prior art and thus are believed to provide allowable subject matter, subject matter apparently glossed-over by the Examiner.

1. Rejected claim 4 of the application calls for "---forming an etching dimension vernier marker pattern in each die---". This language relates to etch measurement subject matter disclosed in the incorporated by reference companion AFD 550, now U.S. 6,653,214, patent. Nothing in the combination of the Hayama et al. and Morcom et al. references relied upon in the final rejection of claim 4 however discloses such a buried within the wafer, graduated scale, etching dimension vernier marker pattern. Such a pattern is respectfully submitted to be readily distinguished from "--the ridges in Morcom et al." as asserted by the Examiner on page 5 of the Final Rejection. Applicants have discussed this via and dimensioned marker issue at length at page 8 in the 8 previous, January 2004, response, a discussion that is hereby incorporated by reference herein. Thus claim 4 in essence stands as being rejected without benefit of prior art support and is respectfully submitted to be allowable.

2. Rejected independent claim 22 of the application in its ninth paragraph calls for "---exposing wafer thickness-received portions of said front side via hole intrusions metallization---" and recites additional via hole details. Both the absence of true via holes and the absence of in the wafer metallized measuring elements in the prior art relied upon in the Final Rejection appear to mitigate for the allowance of this claim in view of this language.

3. Rejected claim 23 of the application in its second paragraph includes the language "---disposing said via hole intrusions to a first depth dimension into said semiconductor wafer---". Both the absence of true via holes and the absence of in-the-wafer metallized measuring elements in the Prior Art relied upon in the final rejection appear to again mitigate for the allowance of this claim in view of this language.

4. Rejected claim 24 of the application includes the language "---said via hole intrusions first depth dimension are each no more than one hundred micrometers---". The absence of true via holes in the prior art relied upon in the final rejection appear to again mitigate for the allowance of this claim in view of this language.

5. Rejected claim 30 of the application incorporates the language "---comprises covering underside portions of etching-exposed second smaller diameter via hole metallizations with ground plane metal." The absence of true via holes in the prior art relied upon in the final rejection appear to once again mitigate for the allowance of this claim.

6. Rejected claim 31 of the application incorporates the language "---exposing wafer thickness-received portions of said front side-received via hole throughways---". The absence of true via holes in the prior art relied upon in the final rejection appear to once again mitigate for the allowance of this claim in view of this language.

7. Rejected claim 33 of the application incorporates the language "---comprises fabrication of radio frequency circuit die having via aperture-measuring graduated dimension metallic patterns disposed within said via hole throughways in thinned portions of said wafer." Both the absence of true via holes and the absence of in the wafer metallized measuring elements in the prior art relied upon in the final rejection appear to once again mitigate for the allowance of this claim in view of this language.

8. With no via holes present in the prior art relied upon in the final rejection there can be no backside metal contact with via conductor as is expressly recited in claims 1, 22 and 31 of the application.

V. Legal Conclusion and Precedent Considerations

In the above-presented argument applicants have made reference to the legal conclusions of:

1. No viable teaching in suggestion of the asserted combination,
2. Non-analogous art,
3. Teaching away from applicants' invention,
4. Failure to consider all of the limitations of a rejected claim,
5. Destruction of the function of applicants' invention or a concept appearing in a reference document,
6. Failing to provide a reasonable expectation of success,
7. Hindsight in view of applicants' invention.

Even though these conclusions are believed well known in the Patent community and are discussed at length in Chapter 2100 of the Manual of Patent Examining Procedure applicants perceive a duty to include at least the following brief discussions and citations of

support relating to each of these conclusions. These discussions are segregated according to the numbers recited above.

1. With respect to a teaching to combine the Hayama et al. and Morcom et al. references applicants note there is clearly no express reference in either patent document identifying the other document, that the inventors worked in different corporations located on opposite sides of the world, that the two patents are classified in different sub-classes in the U.S. Patent and Trademark Office classification system and that the two patents seek to provide clearly distinguishable different types of electronic devices as has been eluded-to earlier herein. None of these practical considerations therefore appear to add teaching or support for the asserted combination.

Moreover it is notable that the several court cases discussed in section 2143.01 of the Manual of Patent Examining Procedure (May 2004) regarding the issue of a teaching to combine references or a motivation to modify references mostly result in an overturn of the asserted 35 U.S.C. 103(a) combination (i.e., with one recent exception in the 7 cases discussed).

The one recent exception discussed in MPEP section 2143.01 concerns the "nature of the problem to be solved " rationale for combining references and the Ruiz v. A.B. Chance Co. case at 69 USPQ 2d 1686 (March 2004). The two references asserted in combination under 35 U.S.C. 103(a) in this case each addressed the same problem i.e., "how to underpin an unstable foundation of an existing building". Applicants submit the wafer breakage problem addressed in the Morcom et al. patent and the metal sidewalls for a non-etchable chemically inert substrate problem addressed in the Hayama et al. patent do not come within this addressing of the same problem classification. Therefore it is submitted that the Morcom et al. and Hayama et al. references should not be combined for this additional reason.

With respect to the need for a basis or teaching in the references or support for an asserted combination, the United States Court of Appeals for the Federal Circuit has previously for example stated in the case of In re Fritch at 23 USPQ 2d 1780, 1783 that:

> "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined *only* if there is some suggestion or incentive to do so."[13] Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be

> modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.[14] (The patents of) Wilson and Hendrix fail to suggest any motivation for, or desirability of, the changes espoused by the Examiner and endorsed by the Board. (parentheses added)."

The references 13 and 14 in this citation refer respectively to *ACS Hosp. Systems, Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984) and *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Also see Dussalich, Ex Parte (Bd Pat App & Interf 6/9/88) 7 USPQ 2d 1818.

With respect to the applicants' invention the patents of Hayama et al. and Morcom et al. are also believed to "fail to suggest any motivation for, or desirability of, the changes espoused by the Examiner" in support of the 35 U.S.C. 103(a) rejection.

2. With respect to the use of non-analogous art as a basis for support of a 35 U.S.C. 103(a) rejection the Court of Appeals for the Federal Circuit in the decision In re Oetiker at 24 USPQ 2d 1443, 1445 has stated the following:

> "It has not been shown that a person of ordinary skill, seeking to solve a problem of fastening a hose clamp, would reasonably be expected or motivated to look to fasteners for garments. The combination of elements from non-analogous sources, in a manner that reconstructs the applicant's invention only with the benefit of hindsight, is insufficient to present a *prima facie* case of obviousness. There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge can not come from the applicant's invention itself. *Diversitech Corp. v. Century Steps, Inc.*, 850 F.2d 675, 678-79, 7 USPQ 2d 1315, 1318 (Fed. Cir. 1988); *In re Geiger*, 815 F.2d 686, 687, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987); *Interconnect Planning Corp. v Feil*, 774 F.2d 1132, 1147, 227 USPQ 543, 551 (Fed. Cir. 1985)".

3. With respect to the absence of prima facie obviousness under 35 USC 103 where the references teach away from the recitation of an applicant's claims, the Court of Appeals for the Federal Circuit speaking in the In re Fine decision at 5 USPQ 2d 1596, 1598 has stated:

> "In fact, Eads says that the presence of nitrogen is undesirable because the concentration of the titration cell components in the sulfur detector is adversely affected by substantial amounts of nitrogen compounds in the sample. So, instead of suggesting that the system be used to detect nitrogen compounds, Eads deliberately seeks to avoid them; it warns against rather

> than teaches Fine's invention. *See W.L. Gore & Assoc. v. Garlock, Inc.*, 721 F.2d 1540, 1550, 220 USPQ 303, 311 (Fed. Cir. 1983) (error to find obviousness where references "diverge from and teach away from the invention at hand"). In the face of this, one skilled in the art would not be expected to combine a nitrogen-related detector with the Eads system. Accordingly, there is no suggestion to combine Eads and Warnick."

The Court of Appeals for the Federal Circuit additionally referred to the concept of a reference teaching away from a position of rejection in an unquoted part of the In re Gordon decision at 221 USPQ 1125 from paragraph V5 below herein.

4. With regard to a 35 USC 103 obviousness rejection and a failure to consider all limitations in a rejected claim as applicants have asserted herein, it appears fundamental that a full consideration of recited limitations is necessary to support a 35 USC 103 obviousness rejection of a claim. The language of 35 USC 103(a) itself appears to support such full consideration of limitations in its requirement that "the subject matter as a whole would have been obvious at the time the invention was made----"

Nevertheless the Court of Appeals for the Federal Circuit has decided several cases in which the failure to consider a limitation (even a normally unpatentable printed matter limitation) was at issue. A particularly clear recitation on this point which also identifies several other related decisions is found in footnote 8 of the 1981 decision in the case of In re Gulack at 217 USPQ 401, 403 wherein the Court states:

> "The CCPA has considered *all* of the limitations of the claims including the printed matter limitations, in determining whether the invention would have been obvious. See In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974); In re Cavrich, 451 F.2d 1091, 172 USPQ 121 (CCPA 1971). In Royka, 490 F.2d at 985, 180 USPQ at 583, the CCPA, notably weary of reiterating this point, clearly stated that printed matter may well constitute structural limitations upon which patentability can be predicated".

The thrust of the entire Gulack decision also appears relevant to the present discussion.

The In re Miller decision of the Court of Customs and Patent Appeals at 164 USPQ 46, 49 is referred to in the Gulack decision and appears to support the present failure to consider all of the limitations position urged by applicants in the language:

> "The solicitor seeks some support for sustaining the rejection in In re Sterling, 21 CCPA 1134, 70 F.2d 910, 21 USPQ 519, but we find none therein. As we pointed out in In re Jones, 54 CCPA 1218, 373 F.2d 1007, 153 USPQ 77, also cited by the solicitor, the Sterling claims were held

> unpatentable over prior art references. The solicitor seems to urge that we *ignore* the claim limitations to the indicia and legends because they are printed and because printed matter is not patentable subject matter by itself. For reasons indicated above, we reject that argument. The decision of the board affirming the rejection of claims 10-13 is *reversed*".

5. With respect to a combination of references wherein the combination would destroy characteristics or function, the Court of Appeals for the Federal Circuit speaking in the decision of In re Gordon at 221 USPQ 1125, 1127 has stated:

> "The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification. See Carl Schenck, A.G. v. Nortron Corp, 713 F.2d 782, 787, 218 USPQ 698, 702 (Fed. Cir. 1983), and In re Sernaker, 702 F.2d 989, 995-96, 217 USPQ 1, 6-7 (Fed. Cir. 1983), both citing In re Imperato, 486 f.2d 585, 587, 179 USPQ 730, 732 (CCPA 1973)."

> "Indeed, if the French apparatus were turned upside down, it would be rendered inoperable for its intended purpose. The gasoline to be filtered would be trapped in pocket 9, and the water French seeks to separate would flow freely out of the outlet 5. Further, unwanted dirt would build up in the space between the wall of shell 1 and screen 21, so that, in time, screen 21 would become clogged unless a drain valve, such as a pet-cock 13, were re-introduced at the new "bottom" of the apparatus. See In re Schulpen, 390 F.2d 1009, 1013, 157 USPQ 52, 55 (CCPA 1968). In effect, French teaches away from the board's proposed modification."

> "Because the PTO has failed to establish a prima facie case of obviousness, the rejection of claims 1-3 and 5-7 as unpatentable under 35 USC Section 103 must be *reversed*."

The In re Schulpen decision referred to here additionally states at page 55:

> "Rather than being made obvious by the reference, such modification would run counter to its teaching by rendering the apparatus inoperative to produce the disclosed tire patches. It seems plain that the solicitor's suggestion must have originated with appellant's own disclosure and such disclosure, of course, cannot be used against him under 35 USC 103. In re Sandiford, 53 CCPA 1087, 358 F.2d 756, 149 USPQ 301." ....

> "For the reasons stated, it is our opinion that the prior art of record fails to demonstrate that the claimed invention is obvious under the statute. The decision is *reversed*."

6. With respect to a combination of references wherein there is a perceived failing to provide a reasonable expectation of success the Court of Customs and Patent Appeals has stated:

> "The view that success would have been "inherent" cannot, in this case substitute for a showing of reasonable expectation of success. Inherency and obviousness are entirely different concepts. In re Spormann, 530 CCPA 1375, 363 F.2d 444, 150 USPQ 449 (1966); In re Adams, '530 patent CCPA 996, 356F.2d 998148USPQ 742(1966)."

7. With respect to a combination of references wherein hindsight appears to provide an incentive to achieve the asserted combination of references the Court of Appeals For the Federal Circuit has stated (in a quotation reproduced above herein) that:

> "The combination of elements from non-analogous sources, in a manner that reconstructs the applicant's invention only with the benefit of hindsight, is insufficient to present a *prima facie* case of obviousness. There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge can not come from the applicant's invention itself. *Diversitech Corp. v. Century Steps, Inc.*, 850 F.2d 675, 678-79, 7 USPQ 2d 1315, 1318 (Fed. Cir. 1988); *In re Geiger*, 815 F.2d 686, 687, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987); *Interconnect Planning Corp. v Feil*, 774 F.2d 1132, 1147, 227 USPQ 543, 551 (Fed. Cir. 1985)".

These recitations from previous court decisions regarding the legal conclusions recited herein are of course only samples of the relevant patent law concepts. The interests of brevity and conservation of Board of Patent Appeals and Interferences resources suggests present curtailment of such samples.

VI. Miscellaneous and Conclusion Matters

Applicants respectfully submit that the preceding detailed consideration of the primary Hayama et al. and Morcom et al. references and their combination and any resulting holding of agreement by the Board with respect to this combination removes such a substantial portion of support for the Examiner's Final Rejection as to make consideration of the secondary Morcom et al., Kohno et al., Yamada et al. and Matsunami references unneeded and counter productive herein.

Applicants also respectfully submit that the dependent claims of the application not specifically discussed herein are carried as to patentability by the limitations recited in the

independent claims in view of the distinctions over the primary Hayama et al. and Morcom et al. references noted.

Notwithstanding a new reference to the Goldstein '080 patent appearing at the bottom of page 11 of the Final Rejection, applicants understand from the absence of language in specific reliance on this reference and from the replacement of the previously argued Goldstein patent with the "new ground(s) of rejection" including the Hayama et al. patent, as indicated on page 12 of the Final Rejection, that the Goldstein patent is no longer an issue in the present proceedings and is therefore in the continuing interest of brevity is not addressed herein. Distinctions regarding this Goldstein patent are however presented in applicants' January 8, 2004, response to the first Examiner's Action and are hereby incorporated by reference herein to the extent needed.

Applicants have discussed in the above "Grouping of Claims" topic possible "specific distinction" exceptions to a general conclusion that the claims of the application stand or fall together.

The Examiner's Action of Final Rejection includes three references to claim 26 of the application. The first of these references on page 2 of the narrative text appears to acknowledge cancellation of claim 26 in applicants' previous response but is ambegious in sentence structure. The second and third references on page 7 of the narrative text indicate the continued presence of claim 26 in the pending claims. Claim 26 is in fact cancelled in applicants' previous January 8, 2004, response.

Applicants respectfully submit therefore, that the present rejection of claims 1-9, 22-25 and 27-37 is not well founded and fails to meet the prima facie case of obviousness standard associated with 35 U.S.C. 103(a). Reversal of the rejection and allowance of claims 1-9, 22-25 and 27-37 is therefore respectfully solicited.

Respectfully submitted,

Gerald B Hollins

Gerald B. Hollins, Reg. No. 25452
Attorney for Applicants-Appellants

GBHollins
513/255-2838

(9) APPENDIX

Appealed Claims

1. The method of fabricating a backside surface of a wafer of microwave radio frequency circuit die, said method comprising the steps of:

forming an array of via holes of selected location and depth dimension in said wafer of circuit die;

said via holes being located in response to selected microwave radio frequency electrical component locations over said front side surface of said wafer circuit die;

said step of forming an array of via holes being performed during a front side accessing of said wafer of circuit die;

disposing a grid pattern mask on said backside surface of said wafer of microwave radio frequency circuit die;

said grid pattern mask including a backside periphery outline masking for each circuit die of said wafer;

removing a layer of selected thickness from said wafer backside surface, said removing being from exposed backside surface areas intermediate elements of said grid pattern mask;

said removing step leaving recessed valley portions of selected thickness disposed intermediate individual circuit die-strengthening upstanding surrounding bluff masked semiconductor regions in said wafer backside surface and exposing backside portions of said formed front side via holes;

interconnecting front side and back side ground plane microwave radio frequency energy conveying metal conductors of said wafer circuit die by way of metallic conductors traversing said via holes.

2. The method of fabricating a backside surface of a wafer of microwave radio frequency circuit die of claim 1 wherein said wafer has an initial overall thickness between five hundred and six hundred twenty five micrometers and has a final thickness of between twenty five and one hundred micrometers in said removed layer recessed valley portions.

3. The method of fabricating a backside surface of a wafer of microwave radio frequency circuit die of claim 1 wherein said step of forming an array of via holes is performed during one of before fabrication of said microwave radio frequency circuit on said die and after fabrication of said microwave radio frequency circuit on said die.

4. The method of fabricating a backside surface of a wafer of microwave radio frequency circuit die of claim 1 further including the step of forming an etching dimension vernier marker pattern in each die backside surface of said wafer after said step of forming an array of front side via holes.

5. The method of fabricating a backside surface of a wafer of microwave radio frequency circuit die of claim 1 wherein said backside periphery outline masking is disposed in a closed geometric pattern encircling each front side microwave radio frequency circuit die and further including a closed geometric pattern backside annular ring of original wafer thickness semiconductor material surrounding said entire wafer of microwave radio frequency circuit die.

6. The method of fabricating a backside surface of a wafer of microwave radio frequency circuit die of claim 1 wherein said step of removing a layer of selected thickness from said wafer backside surface includes a backside surface etching step.

7. The method of fabricating a backside surface of a wafer of microwave radio frequency circuit die of claim 6 wherein said backside surface etching step comprises a dry gas etching sequence.

8. The method of fabricating a backside surface of a wafer of microwave radio frequency circuit die of claim 7 wherein said backside surface etching step includes one of an inductively coupled plasma and an electron cyclotron resonance fast etching processes.

9. The method of fabricating a backside surface of a wafer of microwave radio frequency circuit die of claim 1 wherein said removing step individual circuit die-strengthening upstanding surrounding bluff masked regions further include a wafer periphery-surrounding annular ring upstanding bluff region.

10. (cancelled)
11. (cancelled)
12. (cancelled)
13. (cancelled)
14. (cancelled)
15. (cancelled)
16. (cancelled)
17. (cancelled)
18. (cancelled)
19. (cancelled)
20. (cancelled)
21. (cancelled)

22. The method of making a thinned semiconductor wafer radio frequency integrated circuit device of damage resistant physical integrity, desirable high frequency electrical characteristics and favorable thermal energy dissipating characteristics, said method comprising the steps of:

fabricating electrical circuit portions of said thinned semiconductor wafer radio frequency integrated circuit device on a frontal side of a nominal thickness semiconductor wafer, each said integrated circuit device being disposed in a separate die location of said semiconductor wafer and including a plurality of contact pads;

forming a plurality of via hole intrusions through said nominal thickness semiconductor wafer in locations registered with selected of said contact pads of said integrated circuit device;

said via hole intrusions being formed from said frontal side of said nominal thickness semiconductor wafer;

metallizing said via hole intrusions, said metallizing including establishing via metal electrical connections with selected of said contact pads;

depositing a mask of grid pattern-defining configuration on said wafer backside surface;

said mask of grid pattern-defining configuration determining a plurality of wafer backside grid cells each aligned in surrounding periphery with one of said wafer frontal surface integrated circuit devices;

removing a controlled thickness amount of semiconductor wafer backside surface semiconductor material within each said backside grid cell, said removing including an etching step and leaving a wafer backside grid pattern of semiconductor material of said semiconductor wafer nominal thickness dimension and leaving a selected thickness remainder amount of said semiconductor wafer nominal thickness dimension material, within each said backside grid cell, supporting each said integrated circuit device;

said removing step also exposing wafer thickness-received portions of said front side via hole intrusions metallization;

said etching step also leaving a wafer perimeter-disposed backside ring of wafer semiconductor material of said semiconductor wafer nominal thickness dimension and integral interconnection with said wafer backside grid pattern of wafer nominal thickness dimension;

said wafer perimeter-disposed backside ring of wafer semiconductor material of said semiconductor wafer nominal thickness dimension and said wafer backside grid pattern of wafer nominal thickness dimension semiconductor material in interconnecting combination adding physical handling-assisting substantial physical integrity and rigidity to said now thinned semiconductor wafer;

covering said thinned semiconductor wafer backside including said wafer backside grid pattern cells with a layer of ground plane metal, said covering including forming metal to metal ground plane electrical interconnections with said via hole intrusions metallization;

mounting said wafer on said frontal surface thereof; and

further processing said wafer during continued frontal surface mounting, said further processing including removing each integrated circuit device die from said wafer by wafer segregation within a lateral extent of a backside grid cell.

23. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said step of forming a plurality of via hole intrusions into said semiconductor wafer includes:

disposing said via hole intrusions to a first depth dimension into said semiconductor wafer; and

wherein said selected thickness remainder amount of said semiconductor wafer nominal thickness dimension material in said step of removing a controlled thickness amount of said wafer backside semiconductor material within each said backside grid cell

comprises leaving a selected thickness remainder amount of said wafer nominal thickness equal to said via hole intrusions first depth dimension into said semiconductor wafer.

24. The method of making a thinned wafer radio frequency integrated circuit device of claim 23 wherein:

said semiconductor wafer of nominal thickness is between five hundred and six hundred twenty-five micrometers in thickness; and

wherein said selected thickness remainder amount of said wafer nominal thickness and said via hole intrusions first depth dimension are each no more than one hundred micrometers.

25. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said radio frequency integrated circuit device is comprised of one of field effect and bipolar junction and heterojunction bipolar transistors.

26. (cancelled)

27. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said depositing step mask is a metallic mask.

28. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said removing step etching comprises an anisotropic etching, dry gas, reactive ion, plasma etching sequence.

29. The method of making a thinned wafer radio frequency integrated circuit device of claim 28 wherein said anisotropic etching, dry gas, reactive ion, plasma etching sequence comprises one of an inductively coupled plasma (ICP) and an electron cyclotron resonance (ECR) high density plasma etching sequences.

30. The method of making a thinned wafer radio frequency integrated circuit device of claim 22 wherein said covering step forming of ground plane electrical interconnections comprises covering underside portions of etching-exposed second smaller diameter via hole metallizations with ground plane metal.

31. The method of fabricating a thinned microwave radio frequency semiconductor wafer of significantly retained original wafer physical strength properties, said method comprising the steps of:

defining an array of circuit die locations and circuit die segregation boundaries across a frontal surface of said semiconductor wafer;

forming a circuit die having a plurality of electrical components and front side-received via hole throughways in each frontal surface circuit die location of said semiconductor wafer;

disposing a mask inclusive of mask elements in registration with said circuit die segregation boundaries across a backside surface of said semiconductor wafer; and

removing wafer-thinning backside selected thickness portions of said wafer from regions intermediate said mask elements and thereby unprotected by said mask;

said removing step leaving a physical strength preserving upstanding integrally interconnected mesa array of original wafer thickness extent in registration with said circuit die segregation boundaries across said semiconductor wafer backside surface and exposing wafer thickness-received portions of said front side-received via hole throughways;

covering said thinned wafer backside with ground plane metal, metal extending through said via hole throughways to said frontal surface of said semiconductor wafer.

32. The method of fabricating a thinned microwave radio frequency semiconductor wafer of significantly retained original wafer physical strength properties of claim 31 wherein said array of circuit die locations and circuit die segregation boundaries defined across a frontal surface of said semiconductor wafer and said upstanding mesa array of original wafer thickness extent across said backside surface each comprise a rectangular grid pattern.

33. The method of fabricating a thinned microwave radio frequency semiconductor wafer of significantly retained original wafer physical strength properties of claim 31 wherein said step of forming a circuit die having a plurality of electrical components and front side-received via hole throughways in each frontal surface circuit die location of said semiconductor wafer comprises fabrication of radio frequency circuit die having via aperture-measuring graduated dimension metallic patterns disposed within said via hole throughways in thinned portions of said wafer.

34. The method of fabricating a thinned microwave radio frequency semiconductor wafer of significantly retained original wafer physical strength properties of claim 33 wherein said mask of said step of disposing a mask inclusive of mask elements in registration with said circuit die segregation boundaries across a backside surface of said semiconductor wafer further includes a mask element peripherally surrounding said wafer.

35. The method of fabricating a thinned microwave radio frequency semiconductor wafer of significantly retained original wafer physical strength properties of claim 31 wherein said step of removing wafer-thinning backside selected thickness portions of said wafer includes a selected one of an inductively coupled plasma (ICP) and an electron cyclotron resonance (ECR) high density plasma etching sequences.

36. The method of fabricating a thinned microwave radio frequency semiconductor wafer of significantly retained original wafer physical strength properties of claim 31 wherein said method further includes segregating said circuit die into individual integrated circuits each exclusive of any portion of said wafer backside integrally interconnected upstanding mesa array of original wafer thickness extent.

37. The method of fabricating a thinned microwave radio frequency semiconductor wafer of significantly retained original wafer physical strength properties of claim 31 wherein said semiconductor wafer is comprised of one of silicon and gallium arsenide semiconductor materials.